WHAT IS CLAIMED IS:

1. A floating point operand testing circuit for identifying a status of a floating point operand, comprising:

an analysis circuit configured to determine the status of the floating point operand based upon data within the floating point operand; and

a result generator circuit coupled to the analysis circuit and being responsive to at least one control signal, the result generator configured to assert a result signal if the floating point analysis circuit indicates the floating point status is of a predetermined format specified by the at least one control signal.

2. The floating point operand testing circuit of claim 1 further comprising an operand buffer coupled to the analysis circuit, the operand buffer configured to supply the floating point operand to the analysis circuit.

3. The floating point operand testing circuit of claim 1, wherein the result generator circuit is responsive to at least one of a plurality of control signals that are asserted when testing the floating point operand for one of a plurality of predetermined formats.

4. The floating point operand testing circuit of claim 1 wherein the data within the floating point operand encodes the status in the predetermined format.

5. The floating point operand testing circuit of claim 4 wherein the predetermined format is from a group comprising not-a-number (NaN), infinity, normalized, denormalized, invalid operation, overflow, underflow, division by zero, exact, and inexact.

6. The floating point operand testing circuit of claim 5 wherein the predetermined format represents one of a +OV status and a -OV status.

7. The floating point operand testing circuit of claim 5 wherein the predetermined format represents one of a +UN status and a -UN status.

8. The floating point operand testing circuit of claim 5, wherein the predetermined format for the NaN comprises a plurality of bits indicative of a predetermined type of operand condition resulting in the NaN status.

9. The floating point operand testing circuit of claim 5, wherein the predetermined format represents one of a positive infinity status and a negative infinity status.

10. The floating point operand testing circuit of claim 5, wherein the predetermined format comprises a plurality of bits indicative of a predetermined type of operand condition resulting in the infinity status.

11. The floating point operand testing circuit of claim 1, wherein the result signal is used to condition the outcome of a floating point instruction.

12. The floating point operand testing circuit of claim 5, wherein the predetermined format represents a combination of at least two of the group comprising not-a-number (NaN), infinity, normalized, denormalized, invalid operation, overflow, underflow, division by zero, exact, and inexact.

13. The floating point operand testing circuit of claim 1, wherein the result generator is further operative to update the result signal to indicate the floating point operand is of an alternative format specified by an updated value of the at least one control signal.

14. The floating point operand testing circuit of claim 13, wherein the alternative format is from a group comprising not-a-number (NaN), infinity, normalized, denormalized, invalid operation, overflow, underflow, division by zero, exact, and inexact.

15. A floating point operand testing circuit for identifying a status of a floating point operand, comprising:

an analysis circuit configured to determine the status of the floating point operand based only on the contents of the floating point operand;

an operand buffer coupled to the analysis circuit and configured to store the floating point operand encoded with the status; and

a result generator circuit coupled to the analysis circuit and being responsive to at least one control signal, the result generator providing a result signal indicative of whether the status of the floating point operand conforms to a predetermined format associated with the at least one control signal.

16. The floating point operand testing circuit of claim 15, wherein the at least one control signal is one of a plurality of control signals asserted in order to test the floating point operand for different status conditions.

17. The floating point operand testing circuit of claim 15, wherein the predetermined format is from a group comprising not-a-number (NaN), infinity, normalized, denormalized, invalid operation, overflow, underflow, division by zero, exact, and inexact.

18. The floating point operand testing circuit of claim 17, wherein the predetermined format represents one of a +OV status and a -OV status.

19. The floating point operand testing circuit of claim 17, wherein the predetermined format represents one of a +UN status and a -UN status.

20. The floating point operand testing circuit of claim 17, wherein the predetermined format for the NaN comprises a plurality of bits indicative of a predetermined type of operand condition resulting in the NaN status.

21. The floating point operand testing circuit of claim 17, wherein the predetermined format represents one of a positive infinity status and a negative infinity status.

22. The floating point operand testing circuit of claim 15, wherein the result generator circuit provides the result signal to a floating point instruction processing device that conditions the outcome of a floating point instruction based upon the value of the result signal.

23. A method for testing a floating point status condition of a floating point operand, comprising:

(a) receiving the floating point operand related to a floating point instruction;

(b) determining the floating point status of the operand from only the contents of the floating point operand;

(c) receiving at least one control signal; and

(d) generating a result signal to indicate whether the status of the floating point operand conforms to a predetermined format associated with the at least one control signal.

24. The method of claim 23 further comprising repeating stages (c) and (d) on the same operand.

25. The method of claim 23 further comprising conditioning the outcome of the floating point instruction based upon the value of the result signal.

26. The method of claim 23, wherein the predetermined format is from a group comprising not-a-number (NaN), infinity, normalized, denormalized, invalid operation, overflow, underflow, division by zero, exact, and inexact.

27. The method of claim 26, wherein the predetermined format represents one of a +OV status and a -OV status.

28. The method of claim 26, wherein the predetermined format represents one of a +UN status and a -UN status.

29. The method of claim 26, wherein the predetermined format for the NaN comprises a plurality of bits indicative of a predetermined type of operand condition resulting in the NaN status.

30. The method of claim 26, wherein the predetermined format represents one of a positive infinity status and a negative infinity status.

31. A computer-readable medium on which is stored a set of instructions for testing a floating point status condition of a floating point operand, which when executed perform steps comprising:

(a) receiving the floating point operand;

(b) determining the floating point status of the operand from only the contents of the floating point operand;

(c) receiving at least one control signal; and

(d) generating a result signal to indicate whether the status of the floating point operand conforms to a predetermined format associated with the at least one control signal.

32. The computer-readable medium of claim 31 further comprising repeating stages (c) and (d) on the same operand.

33. The computer-readable medium of claim 31 further comprising conditioning the outcome of a floating point instruction based upon the value of the result signal.

34. The computer-readable medium of claim 31, wherein the predetermined format is from a group comprising not-a-number (NaN), infinity, normalized, denormalized, invalid operation, overflow, underflow, division by zero, exact, and inexact.

35. The computer-readable medium of claim 34, wherein the predetermined format represents one of a +OV status and a -OV status.

36. The computer-readable medium of claim 34, wherein the predetermined format represents one of a +UN status and a -UN status.

37. The computer-readable medium of claim 34, wherein the predetermined format for the NaN comprises a plurality of bits indicative of a predetermined type of operand condition resulting in the NaN status.

38. The computer-readable medium of claim 34, wherein the predetermined format represents one of a positive infinity status and a negative infinity status.